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Design and Simulation of High Performance DDR3 SDRAM Controller

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ABSTRACT

The latest addition to SDRAM technology is DDR3 SDRAM. DDR3 SDRAM (Double Data Rate Three Synchronous Dynamic Random Access Memory) uses 8n prefetch architecture. The embedded applications which need faster memories like signal processing/networking, image/video processing, digital signalling and controlling; these DDR3 devices are used commonly. DDR3 SDRAM has repetitively advanced over the years to keep up with ever-increasing work out needs. The 3rd generation of DDR memories DDR3 SDRAM that come across these demands in computing and server systems are used for high bandwidth storage of working data of a computer and other automated devices. DDR3 Memory Controller works as the interface amongst DDR3 memory and user and manages the dataflow going to and from the main memory. This paper discusses the overall architecture of the DDR3 controller along with the thorough design and operation of distinct sub blocks. To accomplish high performance at low supply voltage and reduced power consumption, this work presents new functions and defines their executions. The focus of this paper is to minimize the delay and power and thus increasing the device throughput using pipelining in the design.

Keywords: *DDR SDRAMs (Double Data Rate Synchronous Dynamic Random Access Memories), Controller core, DDR3 Architecture, VHDL.*

INTRODUCTION:

As anendless increase in system bandwidths, memory technologies have been upgraded for higher speeds and performance.DDR SDRAM controllers generate very precise sequences of addresses, commands and data while observing a myriad of timing requirements. The next generation family of Double Data Rate (DDR) SDRAMs is the DDR3 SDRAM. DDR3 SDRAMs or Double Data Rate Three Synchronous Dynamic Random Access Memories offer plentiful advantages compared to DDR1 and DDR2. In general, double data rate memory provides source-synchronous data capture at a rate of twice the clock frequency.DDR3 devices provide a 30% reduction in power consumption compared to DDR2, principally due to smaller die sizes and the lower supply voltage. These DDR devices consumes lower power, operating at higher speeds, offer advanced performance (2x the bandwidth), and come in larger densities. DDR3 devices also offer other power conservation modes like partial and self-refresh. DDR3 delivers significant performance and capacity improvements over older DDR2 memory.

Technically, DDR3 SDRAM is a high speed synchronous dynamic random access memory with eight banks [1]. Access to different banks may be overlapped. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation as compared to DDR2 SDRAM uses 4n architecture. Due to diverse signalling voltages, timings, and other factors, the accompanying interface techniques used by DDR3 SDRAM is not directly companionable with any earlier type of random access memory (RAM).

The ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth [2] or peak data rates [3] is the prime benefit of DDR3 SDRAM over its immediate ancestor, DDR2 SDRAM. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). As 64 bits data can be transferred at a time per memory module, DDR3 SDRAM gives transfer rate of (memory clock rate) * 4(for bus clock multiplier)*2(for data rate)*64(number of bits transferred) /8(number of bits/byte).

The structure of this paper is as follows: section II, describes the types of memory controllers, Section III discusses proposed software design architecture, section IV shows the work done till now.Finally, conclusion in section V.

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Types of memory controllers

DDR1 SDRAM Controller

A further advance in SDRAM memory technology is the Double Data Rate-SDRAM, or simply DDR1 was originally referred to as DDR SDRAM or simple DDR. After the DDR2 took its place, DDR became referred to as DDR1. The principle applied in DDR is exactly as the name implies "double data rate." This is achieved by transferring data twice per cycle, i.e., on both the rising and then the falling edge of the clock signal. Earlier memory technology such as SDRAM transferred data after one complete digital pulse as opposed to DDR1 [4]. Figure 1 shows the SDR and DDR data transfer with respect to the clock.

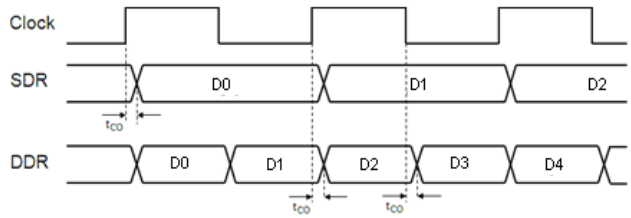

Figure 1: SDR and DDR timing diagram

DDR2 SDRAM Controller

DDR2was introduced in the midst of 2003 as a successor to DDR1. DDR2 SDRAM offers greater bandwidth and density along with a reduction in power consumption. DDR2 allows higher bus speedand requires lower power by running the internal clock at half the speed of the data bus. Like all SDRAM implementations, DDR2 stores data in memory cells that are activated with the use of a clock signal to synchronize their operation with an external data bus.DDR2 runs with power line voltage of 1.8 volts against 2.5 volts for DDR1 SDRAM. Although this represents a drop in voltage of 72%, this would result the power consumed by approximately 50% for the same circuit. DDR2 has also been improved in the operating speed. Prior to working, DDR2 must be initialized first.

DDR3 SDRAM Controller

DDR3 is the next generation memory introduced in the summer of 2007 as the natural successor to DDR2. DDR3 core has an 8n-prefetch (where n refers to the number of banks per rank) as every read access to the memory requires a minimum of 64 bits (8 bytes) of data to be transferred. In addition to the increased data transfer rate memory the voltage level was lowered to 1.5 V to counter the heating effects of the high frequency. With previous versions of RAM, DDR3 is both electrical and physically incompatible. In addition to high frequency and lower applied voltage level, the DDR3 has a memory reset option which DDR2 and DDR1 do not. By using the software reset action, DDR3 allows the memory to be cleared. Other memory types do not have this feature which means the memory state is uncertain after a system reboot. The memory reset feature insures that the memory will be clean or empty after a system reboot. This feature will result in a more stable memory system.

Proposed Software Design Architecture

The DDR3 SDRAM uses double data rate architecture to achieve high-speed operation. The double data rate architecture is 8n-prefetch architecture with an interface intended to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit wide, one-half-clock cycle data transfers at the I/O pins.

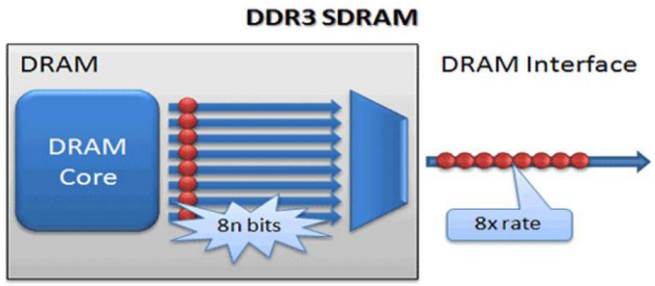

Figure 2: DDR3 SDRAM with 8-bit data rate

Proposed architecure of DDR3 SDRAM

The proposed architecture of DDR3 SDRAM controller is shown in figure 3.

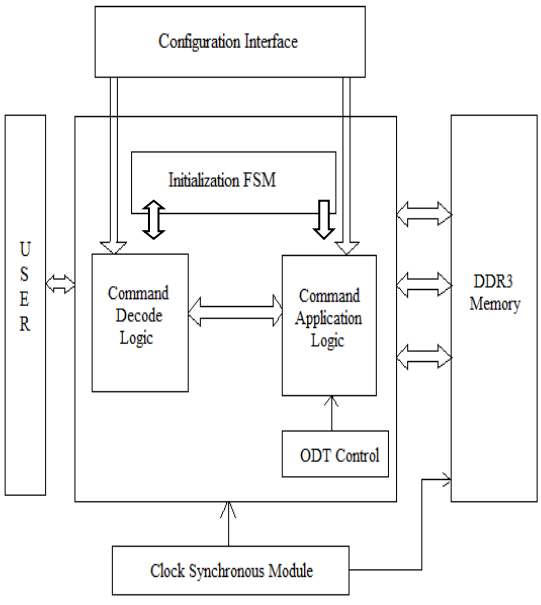

Figure 3: DDR3 SDRAM Controller Block Diagram

DDR3 SDRAM architecture is designed with three stage queue depth command Pipeline Module, Full functional State Machine, ODT (ON-Die Termination) control, clock module,configuration interface, and DDR3 memory.

SDRAM is high-speed Dynamic Random Access Memory (DRAM) with a synchronous interface. The proposed architecture is fully pipelined which allows fast data rates. Double Data Rate Three (DDR3) SDRAM Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability. The core accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The controller core also performs all initialization, refresh and power-down functions.The core uses bank management modules to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time. DDR3 SDRAM is formed with 8 banks and banks are addressed with rows and columns. The number of rows and columns depends on the configuration of the memory and size.

I. ***Full Functional State Machine***

When system leaves the reset state, controller Core of DDR3 SDRAM handles the initialization of the SDRAM. The initialization state machine issues the appropriate sequence of command to initialize the memory devices. It also handles the periodic refresh operations to the SDRAM after initialization. SDRAM Controller provides an interface that allows an external process or logic to drive the SDRAM memory device initialization sequence.

II. ***Burst Length***

This option sets the Burst Length value in Mode Register 0 during initialization. This value remains until the user writes a different value to Mode Register 0.

III. ***Mode Register Set (MRS or EMRS)***

DDR3 SDRAM contains mode and extended mode registers that configure the DDR3 memory foroperation. These registers control burst type, burst length etc. The DDR3 memory controller programs the mode and extended mode registers of the DDR3 memory by issuing MRS and EMRS commands. MRS and EMRS commands can be issued during DDR3 initialization as well as during normal operation as long as the external SDRAM is in idle state.

IV. ***Address and Command Decode***

When the state machine wants to issue a command to the memory, it asserts a set of internal signals. The address and command decode logic turns these into the DDR specific RAS/CAS/WE commands.

V. ***Bank Management Logic***

The bank management logic keeps track the current state of each bank. It can keep a row open in every bank in your memory system. The state machine uses the information provided by this logic to decide whether it needs to issue bank management commands before it reads or writes to the bank. The controller always leaves the bank open unless the users requests an auto-precharge read or write. The periodic refresh process also causes all the banks to be closed.

VI. ***Self-Refresh and Power-Down Commands***

This feature allows you to direct the controller to put the external memory device into a low-power state. There are two possible low-power states: self-refresh and power down. The controller supports both and manages the necessary memory timings to ensure that the data in the memory is maintained at all times.

VII. ***Auto-Precharge Commands***

The auto-precharge read and auto-precharge write commands allow you to indicate to the memory device that this read or write command is the last access to the currently open row. The memory device automatically closes (auto-precharges) the page it is currently accessing so that the next access to the same bank is quicker. This command is particularly useful for applications that require fast random accesses.

VIII. ***DDR3 Dynamic On-Die Termination***

To ensure high signal quality required in a high-speed data transfer system, a processing technology is needed to control signal reflection with greater precision.Dynamic ODT enables the DRAM to switch between HIGH or LOW termination impedance without issuing a mode register set (MRS) command. This is beneficial because it improves bus scheduling and decreases bus idle time.

SIMULATION RESULTS

a) Clock Synchronization Module

Clock synchronization module is used to synchronize the read and write cycle times with the end controller.This parameter specifies the frequency of the memory clock to the DDR3 DIMM module or on-board memory. The allowed range is from 300 to 400 MHz.

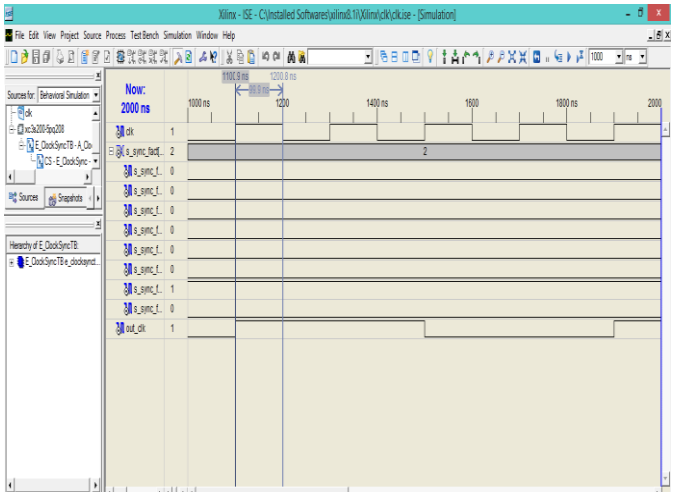

Figure 4: CSM Operation

b) Configuration interface

Configuration interface block consist of a set of registers which are used to store bit values in the form of 0's and 1's so that the functionalities can be implemented in future and the current functionalities can be enabled and disabled.At one time we can activate as many as registers as possible.

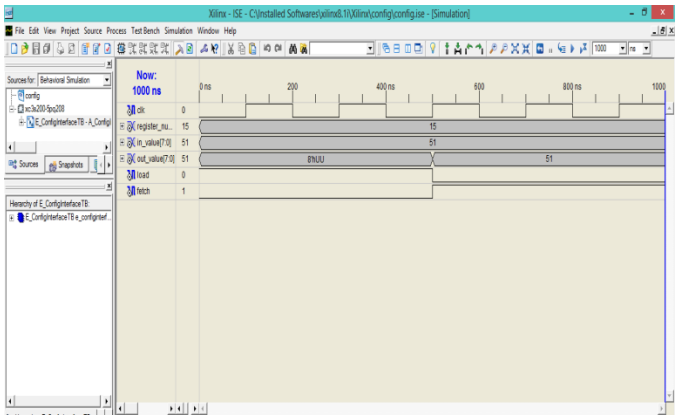

Figure 5: Configuration interface Operation

CONCLUSION

By using the new features of DDR3 SDRAM and using software XILINX 8.1i, the goal is to simplify the proposed design process for DDR3 SDRAM which synchronizes the transfer of data between DDR RAM and external peripheral devices like host computer, laptops and so on.40 percent of projected work is presented here. The design of clock synchronization moduleand configuration interface module is developed and verified using VHDL. The delay comes out to be 9.588nS and the frequency of 104.3 MHz was obtained. The main objective of the paper will be fulfilled by replacing parallel processing by pipelined stages architecture of DDR2 SDRAM Controller to reduce delay.

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